



In re PATENT APPLICATION of

Jun KANAMORI

Group Art Unit: 2814

Continued Prosecution Application of

Examiner: S. Rao

Serial No.: 09/398,189

Filed: September 17, 1999

For: METHOD OF FABRICATING A SEMICONDUCTOR DEVICE WITH SELF-

ALIGNED SILICIDE AREAS FORMED USING A SUPPLEMENTAL SILICON

**OVERLAYER** 

## PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents Washington, D.C. 20231

Sir:

Date: July 12, 2001

Preliminary to the examination of the present Continued Prosecution Application; please enter the following amendments and remarks.

## In the Claims:

Please add new claims 23 and 24 as follows:

-23. A method for fabricating a semiconductor device, comprising

providing a semiconductor substrate which has a silicon region located on a

insulating layer formed in the semiconductor substrate;

forming a metal layer on the silicon region;

performing a first annealing to form a first-reacted silicide region;

forming a supplemental efficon layer on the first-reacted silicide region; and